CLAIMS

1. A Radio Frequency Identification (RFID) tag comprising:

a flexible substrate;

an integrated circuit embedded within the flexible substrate, the top surface of the integrated circuit being coplanar with the flexible substrate;

at least one conductive element formed on the flexible substrate, the at least one conductive element being electrically connected to the integrated circuit, the conductive element serving as an antenna for the RFID tag.

2. The RFID tag of claim 1 wherein the at least one conductive element being electrically connected to the integrated circuit is done through an electrical connection that is capacitive in nature.

3. The RFID tag of claim 1 wherein the at least one conductive element being electrically connected to the integrated circuit is done through an electrical connection that is resistive in nature.

4. The RFID tag of claim 1 wherein integrated circuit comprises at least two interconnection pads.

5. The RFID tag of claim 1 wherein the conductive element comprise at least one of metal particles, organic particles, semiconducting particles.

6. The RFID tag of claim 1 wherein the conductive element is at least one of a printed conductive element, evaporated metal, sputtered metal, plated metal, and a laminated conducting foil.

7. The RFID tag of claim 1 wherein flexible substrate has a width that is one of slightly greater than or substantially equal to the width of the integrated circuit.

8. The RFID tag of claim 1 wherein the RFID tag includes two conductive elements formed on the substrate and wherein the two conductive elements are electrically connected to the integrated circuit on opposite corners or in diagonal corners of the integrated circuit.

9. An RFID tag comprising:

a flexible substrate;

an integrated circuit embedded within the flexible substrate, the top surface of the integrated circuit being coplanar with the flexible substrate, wherein the integrated circuit is embedded within the flexible substrate using a fluidic self assembly (FSA) process;

a planarization layer is formed over the flexible substrate and the integrated circuit

at least one conductive element formed on the flexible substrate, the at least one conductive element being electrically connected to the integrated circuit through at least one via created in the planarization layer, the conductive element serving as an antenna for the RFID tag.

10. The RFID tag of claim 8 wherein the at least one conductive element being electrically connected to the integrated circuit is done through an electrical connection that is capacitive in nature.

11. The RFID tag of claim 8 wherein the at least one conductive element being electrically connected to the integrated circuit is done through an electrical connection that is resistive in nature.

12. The RFID tag of claim 8 wherein integrated circuit comprises at least two interconnection pads.

13. The RFID tag of claim 8 wherein the conductive element comprise at least one of metal particles, organic particles, semiconducting particles.

14. The RFID tag of claim 8 wherein the conductive element is at least one of a printed conductive element, evaporated metal, sputtered metal, plated metal, and a laminated conducting foil.

15. The RFID tag of claim 8 wherein flexible substrate has a width that is one of slightly greater than or substantially equal to the width of the integrated circuit.

16. The RFID tag of claim 8 wherein the RFID tag includes two conductive elements formed on the substrate and wherein the two conductive elements are electrically connected to the integrated circuit on opposite corners or in diagonal corners of the integrated circuit.

17. The RFID tag of claim 8, wherein the RFID tag has a geometry or form factor of a thread tag.

18. The RFID tag of claim 8, wherein the RFID tag has a thickness less than or equal to about 1 mm, a width of less than or equal to about 3 mm, and a length of about 10 mm or greater.

19. The RFID tag of claim 8, wherein the RFID tag assembly is bonded to a nonconductive thread.

20. The RFID tag of claim 19 wherein the nonconductive thread is woven into a fabric.

21. The RFID tag of claim 19 wherein the nonconductive thread is embedded or woven within paper.

22. The RFID tag of claim 19 wherein the nonconductive thread has a distinct appearance that serves a purpose of authenticating the presence of the RFID tag.

23. The RFID tag of claim 19 wherein an adhesive material is used to attach the RFID tag assembly to another item.

24. The RFID tag of claim 19 wherein the RFID tag is deployed in a way that spans three dimensions.

25. The RFID tag of claim 19 wherein the RFID tag includes a visual appearance that makes it difficult to see the RFID tag.

26. The RFID tag of claim 19 wherein the RFID tag includes a visual appearance that makes it easy to see the RFID tag.

27. A method of forming an RFID tag comprising:

depositing an integrated circuit within a receptor in a flexible substrate using FSA;

forming at least one conductive trace on the flexible substrate to simultaneously form an electrical connection to the integrated circuit and form an antenna element.

28. The method of claim 27 wherein the integrated circuit is coplanar with the flexible substrate.

29. The method of claim 27 further comprises forming a planarization layer over the flexible substrate and the integrated circuit, wherein the electrical connection connected to the integrated circuit through at least one via created in the planarization layer.

30. The method of claim 27 wherein the at least one conductive trace being electrically connected to the integrated circuit is done through an electrical connection that is capacitive in nature.

31. The method of claim 27 wherein the at least one conductive trace being electrically connected to the integrated circuit is done through an electrical connection that is resistive in nature.

32. The method of claim 27 wherein the integrated circuit comprises at least two interconnection pads.

33. The method of claim 27 wherein the conductive trace comprise at least one of metal particles, organic particles, semiconducting particles.

34. The method of claim 27 wherein the conductive trace is at least one of a printed conductive element, evaporated metal, sputtered metal, plated metal, and a laminated conducting foil.

35. The method of claim 27 wherein flexible substrate has a width that is one of slightly greater than or substantially equal to the width of the integrated circuit.

36. The method of claim 27 wherein the RFID tag includes two conductive traces formed on the substrate and wherein the two conductive elements are electrically connected to the integrated circuit on opposite corners or in diagonal corners of the integrated circuit.

37. The method of claim 27 wherein the integrated circuit is a NanoBlock integrated circuit.

38. The method of claim 29 wherein the integrated circuit is a NanoBlock integrated circuit.

39. The method of claim 29 wherein the at least one conductive trace being electrically connected to the integrated circuit is done through an electrical connection that is capacitive in nature.

40. The method of claim 29 wherein the at least one conductive trace being electrically connected to the integrated circuit is done through an electrical connection that is resistive in nature.

41. The method of claim 29 wherein the integrated circuit comprises at least two interconnection pads.

42. The method of claim 29 wherein the conductive trace comprise at least one of metal particles, organic particles, semiconducting particles.

43. The method of claim 29 wherein the conductive trace is at least one of a printed conductive element, evaporated metal, sputtered metal, plated metal, and a laminated conducting foil.

44. The method of claim 29 wherein flexible substrate has a width that is one of slightly greater than or substantially equal to the width of the integrated circuit.

45. The method of claim 29 wherein the RFID tag includes two conductive traces formed on the substrate and wherein the two conductive traces are electrically connected to the integrated circuit on opposite corners or in diagonal corners of the integrated circuit.

46. The method of claim 29 wherein the planarization layer comprised of a polymer.

47. The method of claim 29 wherein the conductive trace is formed using at least one of screen printing, ink jet printing, and extrusion printing.

48. The method of claim 29 wherein the conductive trace is formed by a subtractive patterning method.

49. The method of claim 48 wherein the subtractive patterning method includes at least one chemical etching, laser ablation, and mechanical removal.

50. An RFID tag comprising:

a flexible substrate;

an integrated circuit embedded within the flexible substrate, the integrated circuit having a top surface that is coplanar with the flexible substrate;

conductive elements formed on the flexible substrate and electrically connected to the integrated circuit, the conductive elements also serving as an antenna for the RFID tag; and

wherein the conductive elements are formed on a top surface and bottom surface of the substrate, and wherein an electrical connection is provided to connect the conductive element on the bottom surface to the integrated circuit.

51. The RFID tag of claim 50 further comprises a planarization layer formed over the flexible substrate and the integrated circuit and wherein the electrical connection is formed through at least one via hole in the planarization layer.

52. The RFID tag of claim 50 wherein the electrical connection are formed by electrical connection around at least one side of the flexible substrate.

53. The RFID tag of claim 50 wherein the conductive elements formed on the top surface and on the bottom surface are connected through the electrical connection.

54. The RFID tag of claim 53 wherein the conductive elements formed on the top surface and on the bottom surface form electrical loops structures, or inductive elements for the RFID tag.

55. An RFID tag comprising:

an RFID integrated circuit deposited in a flexible substrate;

a first antenna layer coupled to the RFID integrated circuit; and

a second antenna layer coupled to the RFID integrated circuit, wherein the first antenna layer is above the RFID integrated circuit and the second antenna layer is below the RFID integrated, wherein the RFID integrated circuit is coupled to the first antenna layer at the top of the RFID integrated circuit and the RFID integrated circuit is coupled to the second antenna layer at the bottom of the RFID integrated circuit.

56. A method of forming an RFID tag comprising:

combining blocks, each containing a functional component, with a fluid to form a slurry;

dispensing the slurry over a substrate having receptor holes, each of which is designed to receive one of said blocks, wherein the relative size of each hole and

block is such that each block is not axially aligned relative to a perimeter of the receptor holes; and

wherein each block is configured to include a bottom contact pad and a top contact pad that allow the functional component of the block to interconnect to conductive elements formed on the substrate even when each block is not axially aligned relative to the perimeter of the receptor holes.

57. The method of claim 56 wherein the blocks are deposited in the substrate so that they are coplanar with the substrate.

58. The method of claim 56 further comprises forming a planarization layer having vias created therein formed over the substrate and the blocks, the vias allowing for electrical connection to the functional components of the blocks.

59. The method of claim 58 wherein the conductive elements are capacitive in nature.

60. The method of claim 58 wherein the conductive elements are resistive in nature.

61. The method of claim 58 wherein the conductive elements are comprised at least one of metal particles, organic particles, and semiconducting particles.

62. The method of claim 58 wherein the conductive trace is at least one of a printed conductive element, evaporated metal, sputtered metal, plated metal, and a laminated conducting foil.

63. The method of claim 58 wherein each of the blocks is a NanoBlock integrated circuit.

64. The method of claim 58 wherein the conductive elements is at least one of printed conductive elements, evaporated metals, sputtered metals, plated metals, and a laminated conducting foils.

65. The method of claim 58 wherein the substrate has a width that is one of slightly greater than or substantially equal to the width of the blocks.

66. The method of claim 58 wherein the conductive element is formed using at least one of screen printing, ink jet printing, and extrusion printing.

67. The method of claim 58 wherein the conductive element is formed by a subtractive patterning method.

68. The method of claim 58 wherein the subtractive patterning method includes at least one chemical etching, laser ablation, and mechanical removal.